In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown.

1   1.   (Currently Amended) A computer system comprising:

2   a main memory device; and

3   a memory controller, coupled to the main memory device, including:

4   a first queue to store packets that are to be transmitted from the memory

5   controller to the main memory device;

6   a scheduler that includes a slot-based controller, wherein the slot-based

7   controller is adaptable to launch a first packet from the first queue that straddles a

8   first fixed packet slot and a second fixed packet slot.

1   2.   (Currently Amended) The computer system of claim 1 wherein the packet launch

2   position of the first packet is advanced one half of a slot position relative to the second

3   fixed packet slot.

1   3.   (Currently Amended) The computer system of claim 1 wherein the first packet is

2   tagged with an attribute that indicates that the packet is straddling the first fixed packet

3   slot and the second fixed packet slot.

1   4.   (Original)   The computer system of claim 3 wherein the attribute is a Rambus

2   clock offset.

1   5.   (Currently Amended) The computer system of claim 1 wherein the first packet is

2   a Rambus control packet.

1   6.   (Currently Amended) The computer system of claim 1 wherein the memory

2   controller further comprises a Rambus Asic Cell (RAC)~~, wherein the RAC interfaces~~ to

3   interface with <u>the main memory device via</u> a high frequency expansion channel.

1   7.   (Currently Amended) The computer system of claim 6 wherein the <u>memory</u> ~~slot~~

2   ~~based~~ controller <u>further</u> comprises:

3   ~~a scheduler;~~

4   a rules checker coupled to the scheduler;

5   ~~a future packet queue coupled to the scheduler and the rules checker;~~ and

6   a ~~past packet~~ <u>second</u> queue coupled to the ~~future packet~~ <u>first</u> queue, the scheduler

7   and the rules checker.

1   8.   (Currently Amended) The computer system of claim <u>7</u> 6 wherein the rules

2   checker uses entries in the ~~past packet~~ <u>second</u> queue to validate future slot choices for the

3   scheduler.

1   9.   (Original)   The computer system of claim 7 wherein the ~~past packet~~ <u>second</u>

2   queue and the ~~future packet~~ <u>first</u> queue are unidirectional shift registers.

1   10.   (Currently Amended) The computer system of claim 7 wherein the <u>memory</u> ~~slot~~

2   ~~based~~ controller further comprises packet driving logic coupled to the RAC and the

3   scheduler <u>to interface with the RAC</u>.

1   11.   (Currently Amended) The computer system of claim 6 <u>wherein the memory</u>

2   <u>controller</u> further <u>comprises</u>~~comprising~~:

3   an expansion channel coupled to the RAC~~within the memory controller; and~~

4   a repeater coupled to the expansion channel.

1   12.   (Currently Amended) The computer system of claim 11 <u>wherein the main</u>

2   <u>memory device comprises</u>~~further comprising~~:

3   <u>a repeater coupled to the expansion channel;</u>

4   a stick channel coupled to the repeater; and

5   a plurality of memory devices coupled to the stick channel.

1   13.   (Original)   The computer system of claim 12 wherein the memory devices are

2   Rambus Dynamic Random Access Memories (RDRAMs).

1   14.   (Original)   The computer system of claim 11 further comprising a plurality of

2   memory devices coupled to the expansion channel.

1   15.   (Currently Amended) A memory controller comprising<u>:</u>

2   <u>a first queue to store packets that are to be transmitted from the memory controller</u>

3   <u>to the main memory device;</u>

4   a scheduler ~~a slot-based controller adaptable~~ to launch a <u>first packet from the first</u>

5   <u>queue</u> that straddles a first fixed packet slot and a second fixed packet slot.

1   16.   (Currently Amended) The memory controller of claim 15 wherein the <u>first</u> packet

2   launch position is advanced one half of a slot position relative second fixed packet slot.

1   17.   (Currently Amended) The memory controller of claim 15 wherein the <u>first</u> packet

2   is tagged with an attribute that indicates that the <u>first</u> packet is straddling the first fixed

3   packet slot and the second fixed packet slot.

1   18.   (Original)   The memory controller of claim 17 wherein the attribute is a

2   Rambus clock offset.

1   19.   (Currently Amended) The memory controller of claim 15 wherein the <u>first</u> packet

2   is a Rambus control packet.

1   20.   (Currently Amended) The memory controller of claim 15 ~~wherein the memory~~

2   ~~controller~~ further ~~comprises~~ <u>comprising</u> a Rambus Asic Cell (RAC) ~~wherein the RAC~~

3   ~~interfaces~~<u>to interface</u> with <u>a main memory device via</u> a high frequency expansion

4   channel.

1   21.   (Currently Amended) The memory controller of claim 20 wherein the slot-based

2   controller comprises:

3   ~~a scheduler;~~

4   a rules checker coupled to the scheduler;

5   ~~a future packet queue coupled to the scheduler and the rules checker;~~ and

6   a ~~past packet~~ <u>second</u> queue coupled to the ~~future packet~~ <u>first</u> queue, the scheduler

7   and the rules checker.

1   22.   (Currently Amended) The memory controller of claim 21 wherein the rules

2   checker uses entries in the ~~past packet~~ <u>second</u> queue to validate future slot choices for the

3   scheduler.

1   23.   (Currently Amended) The memory controller of claim 21 wherein the ~~past packet~~

2   <u>second</u> and the ~~future packet~~ <u>first</u> queue are unidirectional shift registers.

1   24.   (Original)   The memory controller of claim 21 wherein the slot-based

2   controller further comprises packet driving logic coupled to the RAC and the scheduler.

1   25.   (Currently Amended) A method ~~slot-based controller~~ comprising:

2   ~~a scheduler;~~

3   ~~a rules-checker coupled to the scheduler;~~

4   ~~a future packet queue coupled to the scheduler and the rules checker; and~~

5   ~~a past packet queue coupled to the future packet queue, the scheduler and the~~

6   ~~rules-checker;~~

7   ~~wherein the slot-based controller is adaptable to launch a packet in~~

8   ~~advance of a predetermined packet slot.~~

9   <u>retrieving a first packet from a packet queue; and</u>

10   <u>transmitting the first packet to a memory, wherein the first packet is transmitted</u>

11   <u>straddling a first fixed packet slot and a second fixed packet slot.</u>

1   26.   (Currently Amended) The ~~slot-based controller~~ <u>method</u> of claim 25 ~~wherein the~~

2   ~~advance packet launch is accomplished by straddling the packet on a first fixed packet~~

3   ~~slot and a second fixed packet slot, wherein the first packet slot is designated for a~~

4   ~~previously scheduled packet.~~ <u>further comprising advancing the launch position of the first</u>

5   <u>packet one half of a slot position relative to the second fixed packet slot.</u>

1   27.   (Currently Amended) The ~~memory controller~~ <u>method</u> of claim 25 ~~wherein the~~

2   ~~past packet queue and the future packet queue are unidirectional shift registers.~~ <u>further</u>

3   <u>comprising tagging the first packet with an attribute that indicates that the packet is</u>

4   <u>straddling the first fixed packet slot and the second fixed packet slot.</u>

1   28.   (Currently Amended) The ~~memory controller~~ <u>method</u> of claim 25 ~~wherein the~~

2   ~~slot-based controller further comprises packet driving logic coupled to the RAC and the~~

3   ~~scheduler.~~<u>further comprising accessing a second queue to track previously transmitted</u>

4   <u>packets.</u>